

# Large-Signal Model of a Downstream DC/DC Converter for Analysis and Design of Front-End PFC Rectifier using Computer Simulation

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**Abstract** –For large-signal analysis and design of power supply system with multiple converters, the simulation speed becomes much critical when simulation is employed as virtual prototyping approach. Previously published models for downstream DC/DC converters at the power semiconductor switch level or even the power stage level can hardly meet this requirement. This paper proposes a model that can accurately emulate the input characteristics of downstream DC/DC converters under low frequency small-signal situation or large-signal process. The model is very simple, which makes simulation very fast, therefore can greatly facilitate the design and verification of front-end PFC voltage loop compensator, and the analysis and design of many PFC transient issues in distributed power systems.

**Keywords**- large-signal model;DC/DC converter; power factor correction; computer simulation; distributed power system

## I. INTRODUCTION

In the analysis and design of power electronics converters, small-signal models have been widely and effectively used. Investigations on small-signal issues can easily be accomplished manually or sometimes with the help of computer simulation, according to well-established theories based on small-signal models [1,2]. But for large-signal behavior, so far there is no effective analytical method. Average models can be used to deal with large-signal issues, but it's always very difficult as long as people try to characterize the analysis and design into theoretical conclusions like what has been done for the small-signal behavior [3,4]. This is mainly because usually power electronics converters are

still quite complicated nonlinear systems even under the average model description and by now we have no effective analytical theory for complex nonlinear systems. Therefore computer simulation is still the only approach to large-signal issue investigation so far.

However, to investigate the large-signal interactions among cascaded or paralleled converters in a distributed power system (DPS), time-domain simulations based on full time-domain switching model or even average model are very time-consuming and sometimes have convergence problems, because the system under investigation is very complicated as multiple converters are involved. A typical case is the system composed of an AC/DC Power Factor Correction (PFC) converter and a downstream DC/DC converter as shown in Fig.1. The behavior of the downstream DC/DC converter is very critical to not only the voltage loop compensator design of the PFC converter but also the analysis and design of the PFC converter for many large-signal situations, such as output voltage hold-up ability, input line voltage drop out and brown out, inrush current during start-up, and start-up sequencing process etc. . The time-domain simulation of these situations will be very time-consuming if both converters are emulated by full switching models or even if the downstream DC/DC converter is described by an average model. This is made much worse when there are multiple downstream DC/DC converters. This problem is especially critical to the *virtual prototyping* concept proposed in [5,6], where for each performance specification a significant number of time domain simulations may be run to verify or test the design or help to select the optimum parameters.

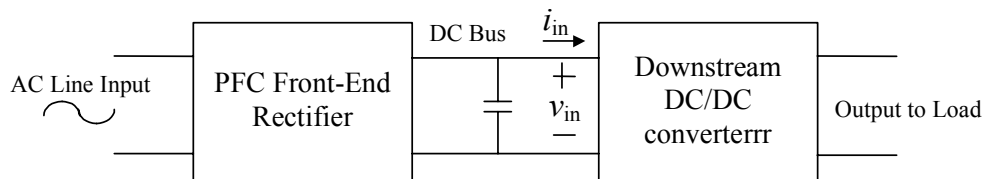


Figure 1. The system composed of a front-end PFC rectifier and a downstream DC/DC converter

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This paper proposes a large-signal model for computer simulation of downstream DC/DC converters to facilitate the analysis and design of front-end AC/DC converters using power factor correction (PFC). As is shown through simulation results and hardware experiments, the proposed model has the following two merits:

- It can accurately emulate the input characteristics of downstream DC/DC converters when the input DC voltage is under low frequency small-signal situation or large-signal process;
- It's very simple, only consisting of several linear and nonlinear components, therefore when incorporated as the load of a front-end PFC converter it can facilitate a much faster simulation than using the detailed DC/DC power stage and control circuit based on a full switching model.

These merits make it very suitable to be used in the design and verification of front-end PFC voltage loop compensator, and the analysis and design of many PFC transient issues in distributed power systems (DPS), which include output voltage hold-up, input line voltage drop out and brown out, inrush current during start-up, and start-up sequencing etc.. It would also be very effective for the investigation of large-signal issues in DPS systems with multiple front-end PFC modules and multiple downstream DC/DC modules connected through a high voltage DC bus.

## II. PROPOSED MODEL

Fig.2 shows the proposed model, which emulates a downstream DC/DC converter feeding a constant resistive load. S is a voltage-controlled switch, controlled by an on/off signal, and  $R_{PWL}$  is a piece-wise-linear (PWL) resistor.

### A. For the Normal Operation (Other Than Start-up and Shut-down)

When the DC/DC converter is in its normal operation mode, the proposed model is actually simplified to just a PWL resistor with the same characteristics as  $R_{PWL}$ . Fig.3 shows the V-I characteristics of  $R_{PWL}$  for a 1kW/400V input DC/DC converter, with maximum input voltage  $V_{in-max}$  as 450V and minimum

input voltage  $V_{in-min}$  as 300V. It consists of three parts. The part between  $V_{in-min}$  and  $V_{in-max}$  is the normal regulation part (or negative resistance part), where the DC/DC converter regulates its output voltage at a constant value therefore its output and input power is also constant. Here the constant power curve is actually approximated by several consecutive linear segments. The part between 0 and  $V_{in-min}$  is the constant resistance part, where the DC/DC converter operates at its maximum duty ratio therefore its output voltage decreases as input voltage decreases. At input voltages greater than  $V_{in-max}$  the converter will eventually fail in a very low impedance mode as switching power semiconductor devices begin to breakdown. This behavior is modeled by a very steeply rising current for excessive input voltages.

All the above is based on the following observations:

Because of the low band-width voltage loop of the PFC and the large capacitor across the 400V bus, to which the input of the downstream DC/DC converter is connected, the variation of this input voltage  $V_{in}$  will be very slow;

The response of the downstream DC/DC converter to the input voltage variation is relatively fast. Up to certain frequency (hereby defined as  $f_R$ ), no matter under small-signal variation or large-signal process, it will behave either as a pure negative resistor when  $V_{in}$  is greater than  $V_{in-min}$ , or as a pure positive resistor when  $V_{in}$  is less than  $V_{in-min}$ ;

Since frequency range of input voltage variation is much smaller than  $f_R$ , no information will be missed if this model is used to assist investigation of front-end PFC circuit behavior, except the very high frequency interactions.

### B. For the Start-up and Shut-down Operation

The behavior of the downstream DC/DC converter is very important to any front-end transient that causes a very large-signal variation of the DC bus voltage  $V_{in}$ . If this large-signal variation of DC bus is large enough, it can trigger the soft start-up or hard shut-off of the DC/DC converter. And the soft start-up and hard shut-off of the DC/DC converter would in-turn greatly affect the front-end transient. Therefore, an accurate emulation of the start-up and shut-down operation of the downstream DC/DC converter is very critical.

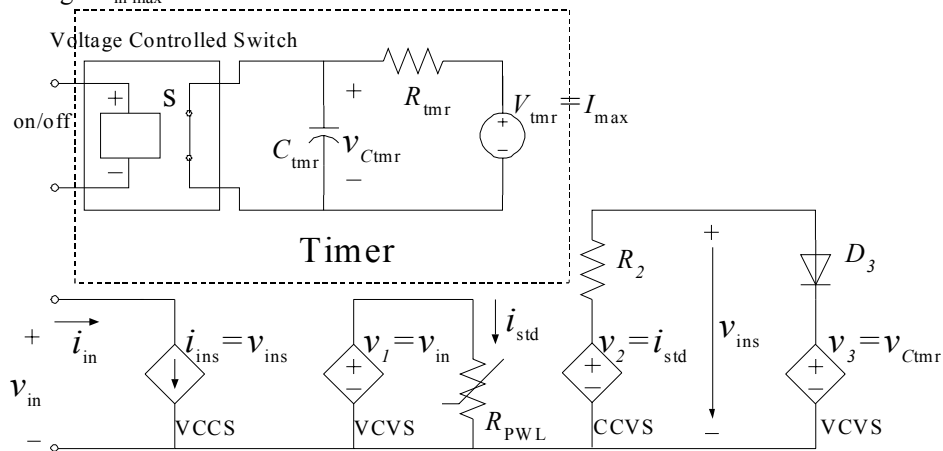


Figure 2. The proposed model of downstream DC/DC converter

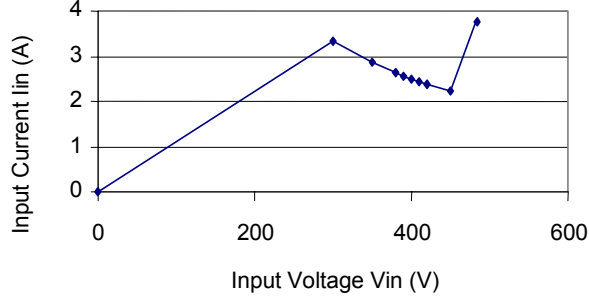


Figure 3. The input V-I characteristics of a 1kW/400V input DC/DC converter

As for the proposed model in Fig.2, the emulation of the start-up and shut-down operation is based on the following observations from the engineering practice:

The transient waveform of the input current during start-up should be exponential, ramp, or any required shape to emulate the “soft start” of different DC/DC converters governed by different control chips; (This could be realized by a timer circuit as shown in the upper part of Fig.2;)

After the start-up, the steady-state waveform and value of the input current is determined by the input voltage and the above-mentioned PWL resistor;

During start-up, when the soft-start transient waveform reaches the steady-state value, the input current should be clamped at that value. And this transient should not happen any more until the DC/DC converter is shut off and started again;

The input current should be controlled by the on/off signal. Signal transition from “off” to “on” triggers a soft start-up transient, and an “off” signal forces the input current to zero.

Fig.4 briefly illustrates the operating principle of the proposed model. The timer circuit in Fig. 2 is for emulating the exponential input current waveform. The timer circuit for emulating other shapes of waveform can also be realized easily with simple components.

### III. APPLICATION IN THE FRONT-END PFC VOLTAGE COMPENSATOR DESIGN

Simulation results of incorporating this downstream DC/DC converter model show that it's very effective in the front-end PFC voltage loop performance analysis and

compensator design. As previously mentioned, this model is actually acting as a constant power load in the normal regulation mode. According to the small-signal compensator design method for the front-end PFC [7], whether the load of the PFC converter acts as a constant resistor or a constant power load will greatly influence the selection and parameter design of the voltage loop compensator in PFC. In other words, using the same compensator, PFC will demonstrate different voltage loop performance depending on the type of load. The simulation results in Figs. 5 and 6 illustrate this difference. These are the results of a 1kW single-switch boost CCM mode PFC starting with the initial voltage of  $v_{in}$  (which is also the DC capacitor voltage) as 360V, operating at 100kHz switching frequency. The current  $i_{PFcin}$  is the current right after the diode bridge rectifier. Fig.5 shows the resulting transient with a pure resistive load, while Fig. 6 shows the resulting transient with the proposed DC/DC converter model. The time constants and steady-state values are very different in these two cases. On the other hand, the CPU time for these two simulations is almost the same. This verifies the simplicity of the proposed model.

### IV. APPLICATION IN THE FRONT-END PFC TRANSIENT ANALYSIS AND DESIGN

Simulation results also show that the proposed model is very effective in the transient analysis and design for the front-end PFC converter. Fig.7 just shows an example of the start-up of a conventional single switch boost PFC converter connected with a downstream DC/DC converter. The line voltage is 110V at 60Hz and the bulk cap is 560 $\mu$ F. To look at the transient analysis and design of PFC, the full time-domain switching model is used for the PFC working at 100kHz switching frequency. The proposed model is used for the downstream DC/DC converter feeding a 1kW resistor load. The DC bus voltage is 400V. The  $v_{DDOK}$  signal is generated through an auxiliary circuit to indicate whether the DC/DC converter is in normal regulation mode.

The simulated waveforms clearly show the three consecutive intervals during the start-up sequencing of the front-end PFC connected with a downstream DC/DC converter:

Interval 1 (from 0ms to 70ms in Fig.7): Line voltage comes in and the bias power for the control circuit is not up yet. Therefore none of the switching devices is working in this interval. The bulk cap voltage  $v_{in}$  (input voltage for the downstream DC/DC converter) is charged up gradually to around the peak value of the line voltage through the diode bridge.

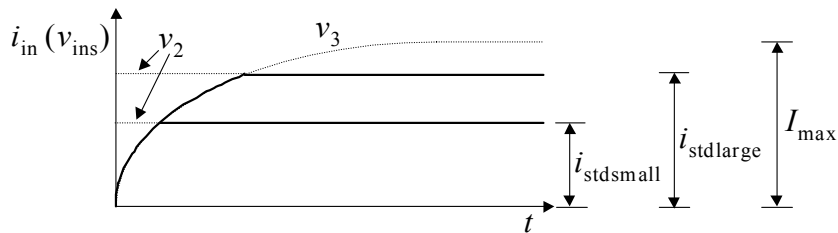


Figure 4. The transient waveform of the proposed model during start-up

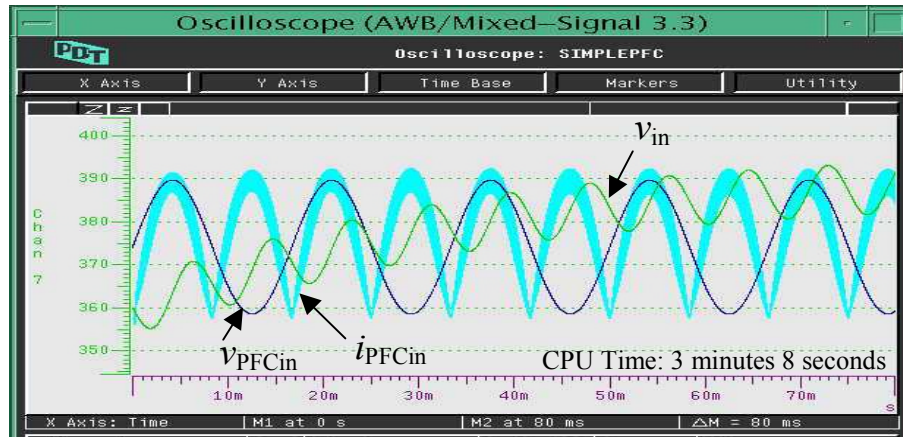


Figure 5. Simulation results for PFC voltage compensator design with a linear resistor model

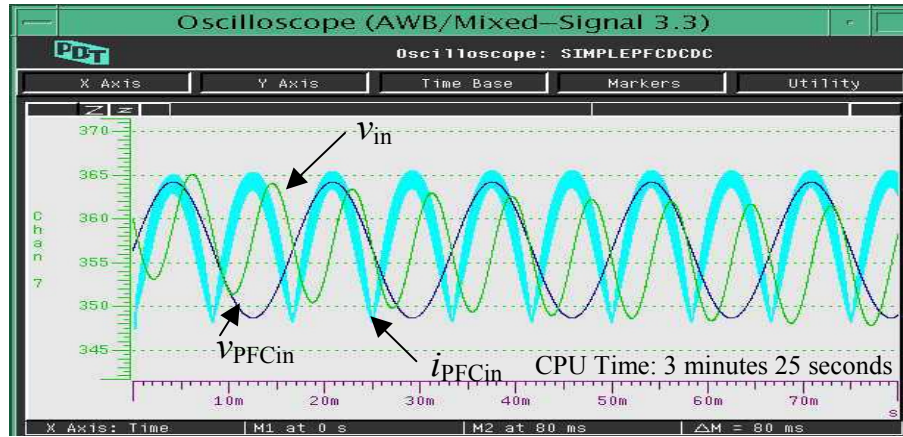


Figure 6. Simulation results for PFC voltage compensator design with the proposed model

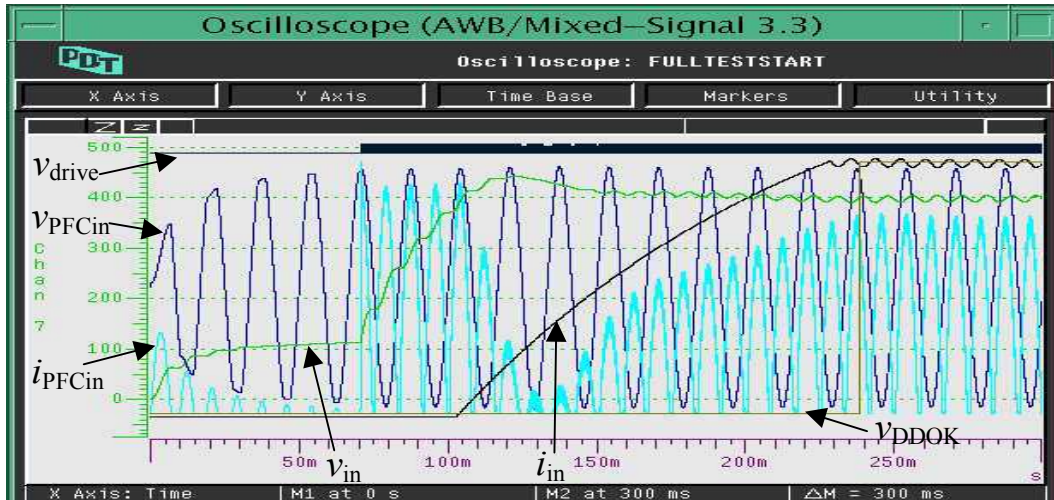


Figure 7. Simulation results for the start-up of the front-end PFC with the proposed model for the downstream DC/DC converter

Interval 2 (from 70ms to around 110ms in Fig.7): After a certain intentionally set time delay in interval 1, the bias power is up and brings up the control chips. The boost PFC then starts to work and charges the bulk cap from the line voltage peak to 400V. At the end of this interval, as  $v_{in}$  becomes larger

than 380V, the soft start-up process of the downstream DC/DC converter is started.

Interval 3 (from 110ms to around 240ms in Fig.7): overshoots and then is regulated around 400V. And then the

input current of PFC follows the soft-start of DC/DC converter and gradually reaches the steady-state level.

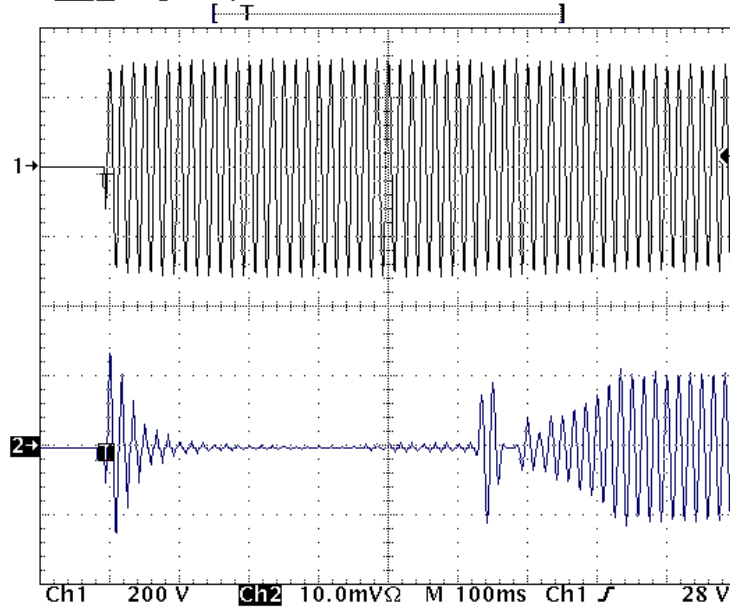
### V. EXPERIMENTAL VERIFICATION

Experimental tests were carried out to further verify the effectiveness of the proposed model. Fig.8 shows some of the

measured waveforms during the experiments. The tests were done on a commercial 1kW front-end converter consisting of a single-phase boost PFC converter and a downstream DC/DC converter.

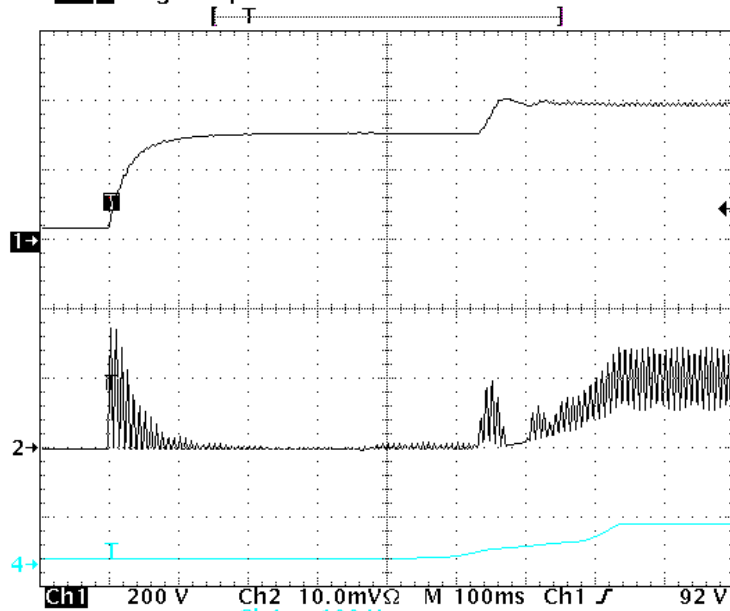
Some parameters in the tests are as follows:

Tek Stop: Single Seq 500 S/s



(a)

Tek Stop: Single Seq 500 S/s



(b)

Figure 8. Experimental results for the start-up of the front-end PFC connected with the downstream DC/DC converter

(a) Input waveforms of the PFC converter: 1 -  $v_{PFCin}$ , 2 -  $i_{PFCin}$  at the AC side;

(b) Input waveforms of the downstream DC/DC converter: 1 -  $v_{in}$ , 2 -  $i_{in}$

- Input line: 220V/60Hz;
- Bulk cap: 660 $\mu$ F (two 330 $\mu$ F caps paralleled connected through a jumper);
- Load resistor: 800W.

Compared with the simulated waveforms in Fig.7, the experimental waveforms in Fig.8 exactly match the time frame, the start-up sequencing, and the wave shape of the three intervals in Fig.7. Notice that the input current of the PFC in the measured waveform was taken at the AC side. And the only big difference is in the input current waveform of the DC/DC converter. There is inrush during the charging up of bulk cap and large ripple in the measured waveform. That was because in the experimental tests the actual input current of the DC/DC converter could not be probed and the measured current waveform is actually the current through the jumper between the two bulk caps.

## VI. CONCLUSION

A large-signal model of downstream DC/DC converter is proposed to facilitate the analysis and design of front-end AC/DC converters with power factor correction (PFC) using computer simulations.

As illustrated by theoretical analysis, demonstrated by computer simulation, and verified by hardware experiments, the proposed model can accurately emulate the input characteristics of downstream DC/DC converters under low frequency small-signal situation or large-signal process. On the other hand the model is very simple, thus can facilitate a much faster simulation than using the detailed DC/DC power stage and control circuit based on a full switching model or even the average model.

The proposed model is very suitable in the design and verification of front-end PFC voltage loop compensator, and the analysis and design of many PFC transient issues in distributed power systems (DPS). It would also be very effective for the investigation of large-signal issues in DPS systems with multiple front-end PFC modules and multiple downstream DC/DC modules connected through a high voltage DC bus.

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