High-Temperature, High-Density Packaging of a 60kW Converter for >200°C Embedded Operation*

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Abstract: **This paper describes the design of a 60kW, actuator motor drive using high temperature SiC devices. Power JFET devices are selected for high-frequency performance and high density. High-density packaging uses an aluminum conductor, AlN substrate and AlSiC combination to minimize dissimilar interfaces. The forced air-cooled design provides >1.1kW/cu.in.**

I Introduction

This project addresses application of silicon carbide (SiC) semiconductor technology to power converters used in areas, such as commercial and military power converters and actuator controllers. Key enabling issues for military applications are size, weight and efficiency of the power electronics. SiC has the potential to provide up to a 5-fold reduction in converter volume if high-temperature, high-frequency power electronics can be implemented.

Higher frequency operation reduces the size of the passive components and, thus, the system volume. Higher operating temperatures allow a larger temperature difference between the heat sink and cooling fluid, which increases radiator effectiveness and decreases size. Silicon devices are limited to 150ºC junction temperature prior to de-rating; whereas SiC devices can operate in excess of 400ºC. In addition, SiC devices offer the potential for incorporating power electronics at Point-of-Load (POL), e.g. at the motor or actuator housing, thus greatly reducing system cabling and volume, and provide increased flexibility in equipment arrangement.

Since available SiC semiconductor switch and diode die have current ratings between 5A to 15A at 25ºC, several die are paralleled within a high temperature power module to achieve 60kW.

This project demonstrates the feasibility of producing a complete 60kW air-cooled SiC, 3-phase converter operating at 0.1MHz The converter operates from a 650Vdc bus and in an ambient of 150°C and lower. The power density is approximately 1kW/cm^3, though a higher density is possible with greater thermal optimization. The SiC devices and packaging can operate continuously at 350°C with high reliability. The primary design focus is on providing high reliability at high temperature. This requires a close design integration of materials, packaging and device selection.

II. System Configuration

The converter approach assumes a 650VDC source bus supplied from an Envelope Power Distribution and Protection System (EPDPS). The EPDPS represents conventional power switchgear, power distribution and fault-protection systems and operates within standard temperatures. Any AC-DC conversion will be part of the EPDPS. The converter is designed as a scalable platform.

The converter uses "normally-on" JFET SiC power switching devices. Many types of SiC devices were evaluated and the SiC JFET was chosen, versus a MOS gated device, because of their superior electrical characteristics and manufacturing maturity. These devices are currently being sampled out in industry. They were originally developed for the European rail systems where high breakdown voltage, low $R_{DS\text{-}ON}$ and fast switching are required.

If "normally-off" operation is desired, a low voltage silicon MOSFET would be placed in series with the JFET source. This "Cascode" or source switched configuration takes advantage of the higher temperature capability of heavily doped, low voltage silicon FETs, which can operate past 300°C., to form a switching device.

For this project, JFET devices are used directly in a normally-on converter configuration because of the overwhelming performance, size and weight advantages, including a high quality internal anti-parallel diode. The normally-on converter provides extensive benefits and utilizes the power system configuration to provide an integrated approach. The EPDPS incorporates required staged power-up sequencing for system checking, diagnostics, power management, etc. A normally-on converter requires that the gate drive systems be energized prior to application of the main power. This inherent need is fully supported in the required EPDPS sequencing.

The test system uses a Moog 6DOF25000E Flight Simulator Platform. The converter duplicates the amplifier specification for operation at 20 kHz PWM, 10 kHz current

* This work was co-funded through Navy Contract: N00024-04-C-4133

loop, with a 5 kHz velocity loop. The actuator uses a 3-phase, 12-pole, continuous operation, brushless, in-line servo with a 60 inch stroke. The platform is rated at 25,000 lbs. Load.

III. JFET Characterization and Selection

The primary design challenge is selecting the number of paralleled devices needed based on the packaging reliability for 350°C junction temperature. An optimization routine was developed that included projected JFET performance across temperature, current per device and manufacturing maturity.

Three losses dominate the device in this application: forward conduction, dynamic switching and reverse diode loss. In the selected actuator drive topology, the drive duty-cycle is varying as a low frequency sinusoidal function over time, which allows the use of phase, q, as a variable instead of time. The model for the total power loss is given by

$$P_{loss} = R_{DSON} I_{PK}^2 \frac{(3\pi+8)}{24\pi} + \frac{V_{BUS} I_{PK} T_{SW} F_{SW} K_{SW}}{\pi} + \frac{V_{DS} I_{PK} (4-\pi)}{8\pi} \quad \text{(Eq. 1)}$$

where R_{DSON} is JFET forward on resistance
I_{PK} is peak actuator current
V_{BUS} is the system dc bus voltage
T_{SW} is the cross-over switching time
F_{SW} is the PWM drive frequency
K_{SW} is the *v-i* transition shape factor (0.16 to 0.3)
V_{DS} is the peak off-state switch voltage

Like silicon MOSFETs, SiC JFETs on resistance varies with temperature significantly and must be taken into account. From manufacturers' data, the R_{DS-ON} as a function of temperature, T in Celsius is approximated by

$$R_{DS-ON} = mT + b = 0.001818T + 0.204545 \quad \text{(Eq. 2)}$$

JFET devices also have a helpful current limit behavior. At a critical current the channel resistance moves the device into a linear mode of operation. JFET's routinely utilize this mode as current limiters. From manufacturers' data the I_{MAX} is approximated by

$$I_{MAX} = aT^2 + bT + c = 0.00297T^2 - 1.7933T + 444.8 \quad \text{(Eq. 3)}$$

The SiC JFET, again like Power MOSFETs, has an integral body diode, but there are several structures. No manufacturers' data is available; therefore, the voltage drop from a comparable commercial pn SiC diode is used. This and other values for the model are summarized below.

$V_{D,r}$ – reverse diode drop: 2 V
V_{TO} – threshold voltage : -30V
$V_{DS,r}$ – maximum drain voltage: 1200V
$V_{GS,r}$ – maximum gate-to-source: -50V

The dynamic behavior of the JFET is modeled by the capacitance of the device. Working with the manufacturers, values for C_{DS} and C_{GS} were derived from several measurements. From the capacitance data, it is readily obvious that the SiC JFET had overall lower capacitance when compared to an equivalent n-channel MOSFET or IGBT. The MOSFETs employ a silicon oxide layer, which adds significant capacitance while the SiC JFET capacitance is due to a reverse-biased diode junction. This difference increases significantly the number of SiC devices a gate-drive circuit can drive versus MOSFET drivers. Also, the SiC devices switch much faster.

A SiC JFET SPICE model is now created from the internal JFET SPICE model, and used to simulate the gate-drive circuit behavior and losses. The JFET netlist is

```
.model SiCJFET NJF BETA=0.1 LAMBDA=4m VTO=-17 RD=0 RS=0
+ CGD=1000p M=.3821 PB=1 FC=.5 CGS=880p IS=173.3f N=1 XTI=3
+ KF=37.24E-18 AF=1
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B. Trending

Discussions with manufacturers yielded projections in JFET maturity over time. The present design approach provides a near-in design for a 40kW converter with a 60kW capability when projected 2009 JFETs are used. The physical design would not change. Relative improvement projected to 2009 reduces R_{DS-ON} by 66% and increases the I_{MAX} by 3X.

IV Design Optimization

To determine the number of parallel SiC JFET chips needed, an optimization is performed incorporating the changes in device resistance, maximum allowed current, and technology maturity. The user inputs the Bus Voltage and Motor Rating, which describe the system requirements. Then various parameters of the motor drive topology are calculated. The key parameter is Peak Phase Current, which s is used to determine the power loss in the SiC JFET.

A. Input Parameters

Table-I lists the input parameters to determine the JFET current and number of SiC die needed in be paralleled for the 60kW converter. A 585Vdc Bus Voltage represents a –10% low line value from 650Vdc accounting for any bus sag due to or low frequency ripple. The JFET PWM frequency and Switching Time are FSW and KSW as used in Eq. 1. The

TABLE – I. INPUT PARAMETERS

Bus voltage	585	V
Peak current	136.8	A
Frequency	1.00E+05	Hz
Switching time	1.00E-07	s
Switching constant	0.333	(Valid from 0.167 to 0.333)
Junction Temp	350	C (valid from 25C to 350C)
Keepout	0.2	cm (keep-out distance from die)
R_{jc}	0.175	(C/W)/cm^2 (junction to package)
Year	2009	C (2005 to 2009)

converter is designed for 100kHz PWM operation with 100nsec device switching times. The Switching Constant fine-tunes the switching loss depending on the load and parasitics. A worst case of 0.333 is assumed. The Junction Temperature

sets a maximum value to adjust R_{DS-ON} and I_{MAX} of the SiC JFET. The Keepout is used to set the minimum distance between the die and allows calculating the required surface area covered by SiC chips. R_{jc} is an estimate of junction to case thermal resistance and modified later when packaging is finalized. This also projects the total thermal resistance at the package. The Year adjusts R_{DS-ON} and I_{MAX}.

B. Determination of Die Count

From the input parameters, JFET characteristics are calculated along with power losses versus numbers of paralleled die. The Diode Parameter is for an external diode and set to 1W. Results are excerpted in Table- II.

TABLE – II. OPTIMIZATION RESULTS

Number in parallel	9	10	11
Conduction loss per chip	15	12	10
Switching loss per chip	9	8	8
Diode loss per chip	1	1	1
Total loss per chip	26	22	19
Total loss per module	231	218	207
Total chip area	1.62	1.8	1.98
Total surface area	6.11	6.79	7.47
Total thermal resistance	0.108	0.0972	0.0884
Max module temperature	325	328.8	331.7
Peak current per chip	15	14	12

The target application requires 137A peak current from Table-I, which represents a worst-case continuous requirement. From the results in Table-II, ten (10) die are needed at 14 amps per die and 0.0972 °C/W packaging.

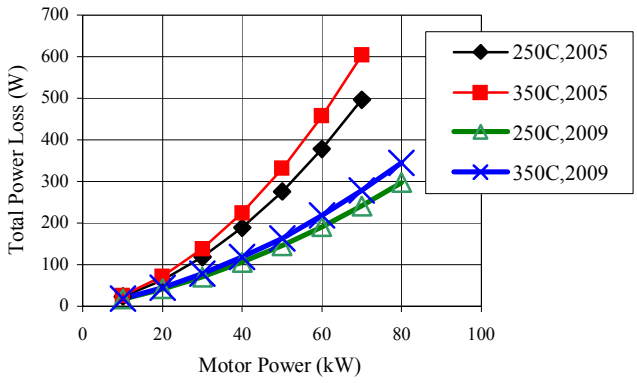

Fig. 1. Total power loss for 10 die v. motor power

Figure 1 shows that a thermal design for dissipating 218W will support 10 SiC JFETs operating in a 40kW converter with 2005 JFET technology. For the same thermal management, the converter can operate at 60kW in 2009. An alternative approach would be to increase the power density at 40kW in 2009 – chart not shown.

V. Gate Drive Development

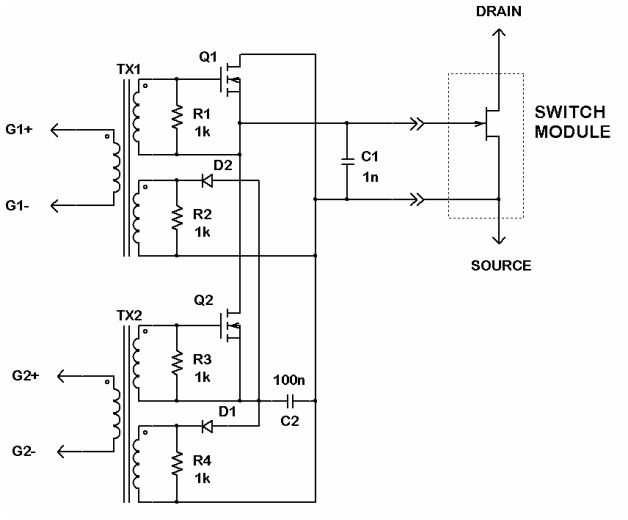

Fig. 2. Gate Drive Design

The gate drive is shown in Fig. 2. The circuit needs to provide electrically isolated high-speed operation, 0 to 100% duty cycle and negative bias.

A. Drive Operation

The drive generates a signal based on the differences between signals G1 and G2 (Fig. 2), also known as a phase difference gate drive circuit. Operation is as follows:

Turn On – When G1 pulses positive, Q1 turns on, C1 is shorted and the JFET V_{GS} goes to 0V. When G1 pulses negative, Q1 turns off; C1 is at 0V V_{GS} at 0V for a period of time while C2 is charged through D2.

Turn Off– When G2 pulses positive, Q2 turns on, C1 is charged to C2 and the JFET V_{GS} is at – V_{C2}. When G2 pulses negative, Q2 turns off, C1 is at – V_{C2} and keeps the JFET off for a period of time while C2 is charged through D1.

0% Duty-Cycle(and Gate Drive pre-charging) – The G1 signal is held at 0V and G2 pulses at some rate to maintain charge on C2. This mode is also used to charge C2, the negative bias, before applying primary power to the 3-phase motor drive H bridge.

100% Duty-Cycle – The G2 signal is held at 0V and G1 pulses at some rate to maintain a charge on C2.

Since Q1 and Q2 are standard power MOSFETs, only 12V is required for the gate drive voltages, G1 and G2. The on-time of the pulses will need to be sufficiently long to assure a JFET has passed through the dynamic switching range. This is critical for turn off where the Miller capacitance could support momentary turn-on if the drive source impedance is not sufficiently low. The C2 must also be sized so that Miller capacitance has little effect during switching. Resistors R1-R4 were required to "snubber" the ringing on the secondary side of the gate drive transformer.

B. Gate Drive Features

There are two unique features to this gate drive. One is the ability to generate a negative bias on the negative pulse of either G1 or G2. This can be done by driving TX1 or TX2 negative or allowing it to "fly back" the voltage. Another

unique feature is the low volt-time product on the drive transformer. The heating of the core is related to the flux-swing. In typical MOSFET/IGBT PWM gate drives the on-time could be as high as 1/'twice switching frequency', e.g. 5 µs for a 100kHz design. In this design, the on-time is 100 ns – a 50 times improvement in ΔB. This allows a reduction in core area and number of turns. Since on-time is low, the added current ramp due to magnetizing inductance is much lower than in standard gate drives.

The gate drive circuitry is required to be as physically close as possible to the JFETs. However, there are thermal limits to the gate drive components lower then the JFETs. The drive will operate at a worst-case 250°C and mounted above the JFET, separated thermally through unique packaging.

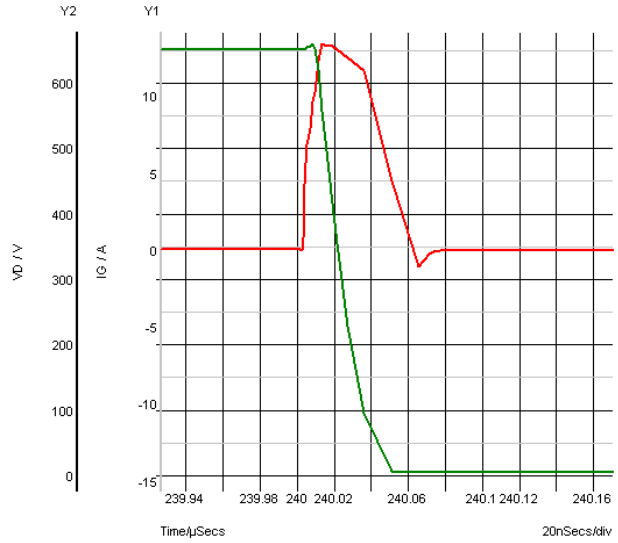

Fig. 3a. JFET Drain voltage and Gate current - Turn-on (20ns/div)

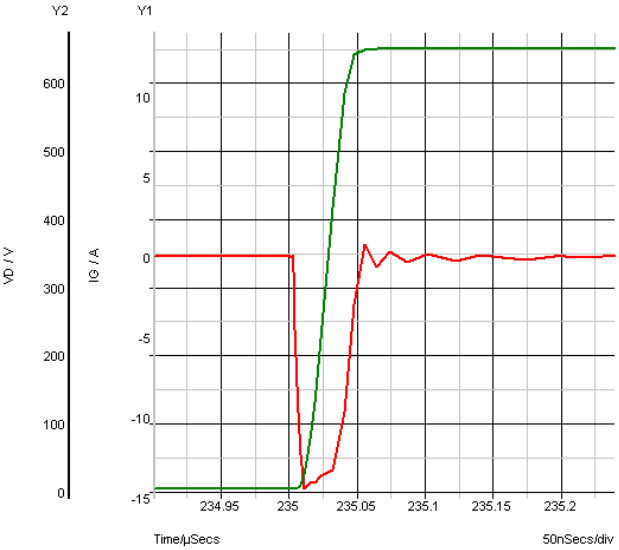

Fig. 3b. JFET Drain voltage and Gate current - Turn-on (50ns/div)

C. Gate Drive Simulation

An extensive gate drive model was created, which includes major parasitics. Simulation results are shown for turn-on and turn-of in Fig. 3a and Fig. 3b, respectively. The results which are based on worst-case parameters, indicate that the optimization cited earlier is more conservative, e.g. in values used for turn-off times of JFETs.

VI. High Temperature Materials Selection

This converter design is unique in that mechanical reliability preceded the electrical design. A paramount requirement is to minimize dissimilarity in material interfaces. Review of packaging approaches lead to a "nearly all" Al (aluminum) approach. This includes Al backed SiC JFETs, AlN (aluminum nitride) and aluminum oxide electrical insulators, Al interconnects (in place of copper), and AlSiC (aluminum silicon carbide) heat sinks. The Al is adequately ductile to act as an excellent stress relief during temperature cycling. Also, Al provides a common metallurgical bonding medium.

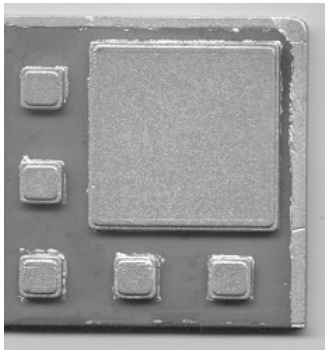

Fig.4 Al/AlN/AlSiC test structure

A. Module Construction

An AlSiC MMC (metal matrix composite) base structure was chosen [1] because of available tailoring of electrical and thermal conductance, and CTE. The AlSiC is considered for two applications: one as a heat sink electrically active (hot) and the other with an AlN ceramic substrate to isolate electrically active conductors. An oxide is grown on masked Al as an electrical isolator. The oxide is grown on other Al structures in the converter to provide electrical isolation with good thermal conductance, and good wear characteristics. Electrically "hot" AlSiC heats sinks are isolated with oxide.

TABLE III. MATERIAL PROPERTIES

	CTE	Thermal Cond.	Electrical Resist.	Young's Modulus	Flexural Strength
	ppm/°C	W/m°C	mW-cm	GPa	$(MPa)_{avg}$
Al/SiC	8	175		220	369
AlN	4.5	100-180		320	300
SiC	3.7	120-490			550
Al	23	240	4.3		
Copper	17	393	1.7		
Gold	14.2	297	2.2		
Silver	19.7	418	1.6	11	

The module structure consisted of Al conductors on AlN substrate on AlSiC. Specifically, in a one- or two-step casting process, a pattern of Al conductor formed on AlN, which is affixed to an AlSiC netshape heat sink. Working with a manufacturer, a test sample was created first created with multiple pads for JFETs and wirebonds, shown in Fig. 4. (A light etch sharpens features.)

Also, using AlSiC for the housing and heat sink allows a ceramic substrate, connectors, and other hardware to be

integrated into the mold, or directly cast into the structure. Connectors that require solder are nickel and gold plated.

B. Aluminum Interconnect

Material properties are given in Table – III.The Al electrical resistance is 2.5X higher than copper and has a 40% lower thermal conductance. Hence, a 2.5X thicker conductor is used for equal power dissipation with a penalty of 40 higher thermal resistance. The thermal resistance is not a large absolute value, and more importantly, the thicker conductor greatly mitigates stresses between components. Both materials approximately double resistance every 100°C.

C. Die Attachment

One of the more significant challenges facing this project was die attach. The SiC semiconductor must be bonded to the AlN substrate with a material electrically conductive, having a high physical resistance to temperature excursion, and imparting little stress on substrate or die during power and temperature cycling. A major question posed was how many die may be reliably mounted on a substrate. Several materials and processes were considered.

Aluminum brazing and ultrasonic welding – aggressive chemistries and physical agitation ruled out aluminum brazing techniques as well as aluminum ultrasonic welding techniques for concern of damage to the SiC semiconductor device.

Thick-film gold – thick-film gold has been used as a die-attach material for SiC devices in the all gold materials system. This material fires at 850°C, has a low electrical resistivity and relatively high thermal conductivity. One issue is the high processing temperature on electrical parameters of the semiconductor, plus the interconnect material must be gold plated to use it effectively. The rigidity of gold also readily translates stress.

Silver-glass composite – Several vendors offer silver/glass pastes for die attach. Two materials were found to be outstanding candidates capable of withstanding and operating at or above 450OC: QMI 2419 and QMI3555R . The QMI3555R was chosen for testing due to its superior thermal conductivity and lower CTE.

The QMI355R is used to attach an Al-metalized SiC power die to both an aluminum substrate and AlSiC substrate. These parts were temperature cycled between –55 and +125°C. The test specimens exceeded 300 temperature cycles without failure. Die sheer strength is much higher than expected. Note that a significant CTE mismatch existed between the 250 micron (10 mil) aluminum skin (on the AlSiC) and the SiC die. This serves to substantiate that the material is performing as advertised, i.e. has significant compliance over the temperature range, and is capable of absorbing the strain between dissimilar materials. The material was selected because it has been shown to be void free, very pliable across the very wide temperature of use, low electrical resistivity, and easy to process.

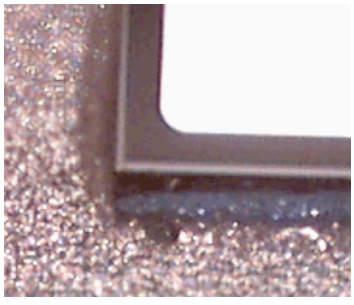

Fig. 5 Die attach test of Silver-Glass

One concern may be silver migration [2]. However, the constraining of silver within glass mitigates most of the migration problem, operation above 100°C eliminates moisture problems and final steps could the surfaces with a high temperature conformal coating. Anodizing the surfaces of any Al or AlSiC stops corrosion or migration.

D. Hermetic Structure and Sealing

If required, an inert high temperature glob top material can be added and, for military applications, the module hermetically sealed to protect the semiconductor device and module interconnects. A cover coating material was investigated and an alumina refractory cement, often used for power wire wound resistors and heaters, was selected. At room temperature the material is a paste, and after application it is cured at room temperature. In the cured state, the material has the properties of alumina ceramic, devoid of outgassing, completely inert, and good to a service temperature of up to 1634°C. The CTE is 4.5 ppm/°C, dielectric strength 270 V/mil, and volume resistivity 1011 Ω-cm.

VI Physical System Design

The physical embodiment of the converter is divided into two levels: a Multi-Chip Power Module (MCPM) representing a “Level-I” packaging approach, and a Power Module and Interconnect Frame (PMIF) representing the ”Level-II” or “Box Level” packaging. The combination provides a power-processing (power amplifier) configuration (converter).

The heat sink of the MCPM is electrically conductive forming an EC-MCPM requiring that the module is electrically isolated from the frame (PMIF). Alumina coatings (“hard anodize”) are used as described in the materials section. The Frame hosts the Module, Gate Drive, converter-bridge circuit interconnects, and connectors to the outside. The entire structure is forced-air cooled. The Frame has two embodiments; a “radial” air-flow design (PMIF-R) with a lower power density and, consequently, lower thermal density of the exhaust air; and a “axial” design (PMIF-A) offering the highest power density with in-line airflow, albeit at much higher thermal density. The first embodiment is featured in this development since it addresses all the Level-II packaging problems and is easier to understand.

A. Module Layout (EC-MPCM)

The thermal analysis showed that a max of 25W can be dissipated in the SiC Switches for a 350°C maximum junction temperature. The electrical analysis shows that 10 SiC devices provide the needed power processing per bridge switch and each device would dissipate 25W. The SiC JFET devices have an inherent anti-parallel diode. Hence, the physical system is partitioned with 1 module per switch having 10 devices per module, yielding six modules per 3-phase converter. The gate-

drive is partitioned to drive 5 SiC devices; requiring two gate-drive circuits per module.

An integrated heat sink/interconnect system for the MCPM was designed. The result is an AlSiC heat sink with captured ceramic having Al traces formed on the ceramic as in Fig. 6. All but the JFETs are created in one/two step process.

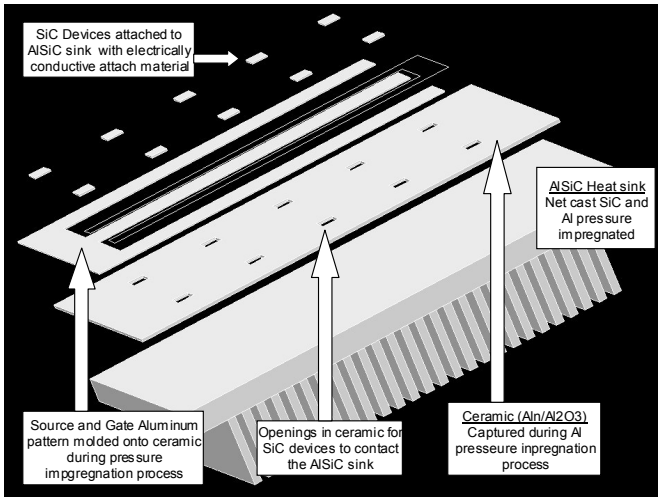

Fig. 6. Module Structure with cast approach

B. Thermal Modeling and Results

A FEM model was built. The module has effectively 10 die attached to an Al skin on the surface of the AlSiC heat sink (heat is electrically hot) with each die producing 21 W of heat. Concurrently an Al interconnect (trace) is mounted to an AlN substrate, which is attached to the AlSiC heat sink by means of a thin aluminum skin.

Air at 400 ft/min cools the heat sink. The flow speed is modeled as constant along the fins. The goal of the analysis presented in this section is to determine the spatial temperature

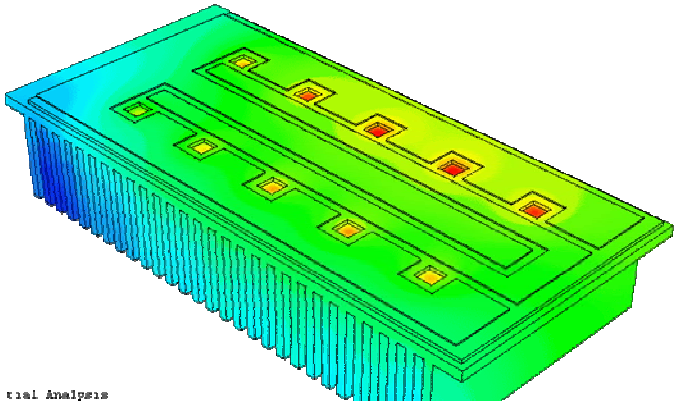

Fig. 7. Thermal profile from FEM analysis

distribution under specified load conditions. A pure (uncoupled) heat transfer analysis is performed. Nonlinearities are included by the temperature dependent material properties. The structure was modeled using quadratic solid elements.

Figure 7 shows the overall temperature distribution. The maximum temperature is 353 C. Asymmetry exists since dies and the Al patterns are not symmetrically located about a centerline.

Figure 8 shows the thermal budget for a single SiC device dissipating 25W on an "Electrically Isolated – MCPM," note the ceramic under the SiC device. The drop across the SiC is about 10°C and across the ceramic is about 20°C. The AlSiC structure is about 30°C (300°C - 270°C).

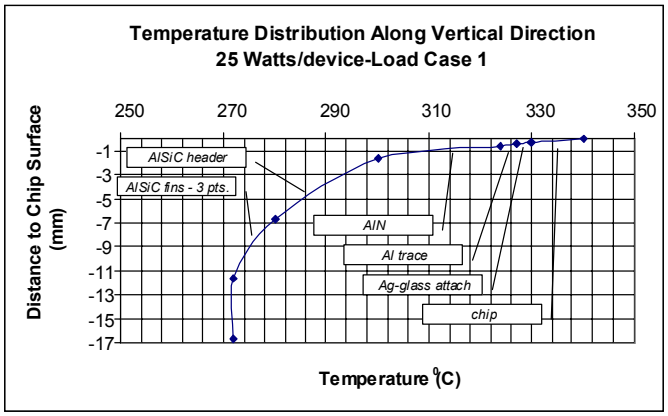

Fig. 8. Thermal budget for an "electrically isolated" MPCM

C. Stress Modeling and Results

The stress analysis used the resulting temperature distribution from the steady-state heat transfer analysis described above. This procedure is termed a sequentially coupled heat transfer-mechanical analysis. Stresses are the result of the combined effect of the coefficient of thermal expansion (CTE) mismatch between the different materials and the prescribed mechanical boundary conditions. The lateral (end) edges parallel to the fins are assumed fixed. This is a rather conservative boundary condition that introduces large stress concentrations along edges.

The prescribed set of boundary conditions together with the CTE mismatch causes the upper plate to deform in

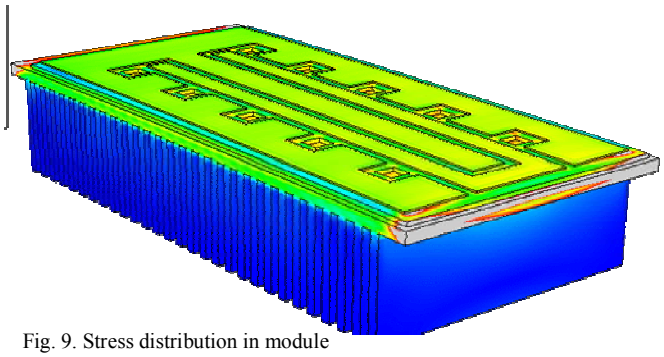

Fig. 9. Stress distribution in module

bending. The following results are shown in terms of the Misses stress distributions. Although in the present model only linear elastic analysis has been performed, the Von Misses stress distribution can be used to predict at least in a qualitative form if yielding or inelastic behavior should be expected.

Fig. 9 shows the overall Von Misses stress distribution. It is clear that the heat sink fins are almost stress free with the

only stressed region located in the region where the geometry changes abruptly.

Finally, Fig.10 shows the stress distribution in the region of the JFET well along the maximum deflection zone. As expected high stresses (close to 800 MPa) are predicted along this region. The large stress value is due mainly to the assumed boundary condition.

The initial analysis identifies high stress regions and needs to be corroborated by the manufacturer. Though stresses

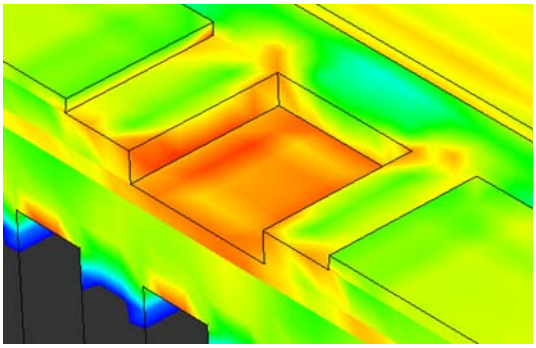

Fig. 10 Stresses in JFET well (JFET not attached)

are reasonable, the final design requires adjustment of AlSiC properties to provide the highest reliability.

D. Final Level-I Module Assembly

The final module assembly adds the two gate drive circuits and thermal barrier on top of the MCPM. The gate drive uses SOI devices fabricated on a thick-film hybrid and operates to a maximum of 200°C. Hence, a thermal break is needed from the MCPM. An interposing glass-ceramic plate provides the thermal break as shown in Fig. 11 to form a single subassembly. The three layers: MCPM, thermal plate, and Gate Drive are secured in the PMIF-R frame with the high temp adhesive (die attach adhesive or the lid sealing cement). Redundant fasteners are added at the end.

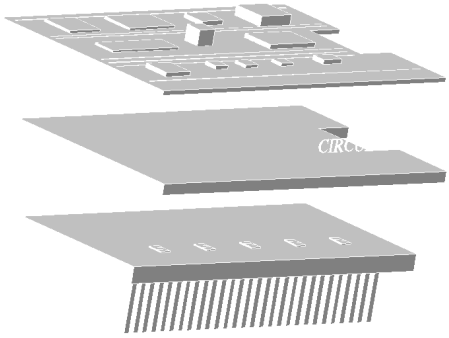

Fig 11. Gate drive, thermal break and MCPM assembly

E. Final Level-II Frame Assembly

The entire power converter is brought together at the box level. The MCPM is electrically hot and therefore, electrically isolated from the frame. Essentially, the electrical isolation barrier is removed from under the JFET and placed at the box level. Needing to incorporate electrical isolation does not inhibit the thermal path under the chip. Also, the entire AlSiC heat sink is involved in electrical current conduction offering a

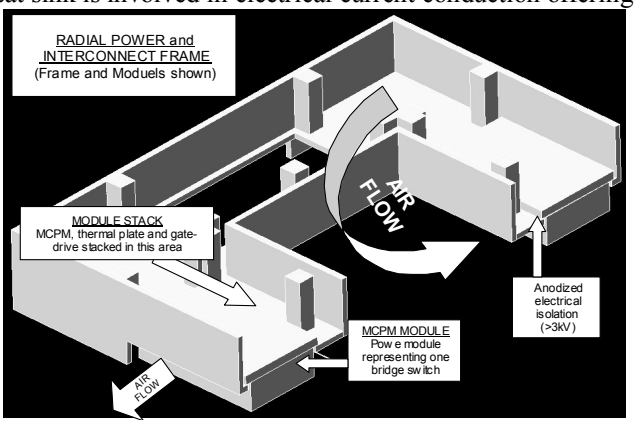

Fig. 12 Lower half frame housing MCPMs, etc.

lower electrical resistance. (Interconnecting 6 bridge switches is interconnecting 6 AlSiC heat sinks.)

Figure 12 shows one of two shells. A second "top" shell mirrors the bottom shell. Air entering the center flows out radially across three pairs of fins. Not shown are slots in the center vertical walls so that force air also flows across the gate drive board and thermal plate. A lid would be attached to cover the contents.

VII CONCLUSIONS

The converter can deliver 150A peak / 60kW from a 650Vdc with a density of 1.1kW/in^3 and 97.2% efficiency. The converter uses SiC JFets with internal anti-parallel diodes. Reliability and thermal management were the primary research drivers. The converter operates from a 650Vdc bus in an ambient of 150°C. The primary SiC devices and packaging can operate continuously at 350°C with high reliability.

Thermal analyses shows a max of 25W can be dissipated per SiC JFET for a 350°C maximum junction temperature. Electrical analysis shows that 10 JFETs provide the needed power processing per bridge switch. Six switches are needed for each 3-phase converter. The SiC JFET devices have the anti-parallel diode inherent in the structure.

ACKNOWLEDGEMENTS

Dr. Birol Sonuparlak at PCC-AFT, Don Hazelmyer at Hybrid Dynamics Inc., Infineon, and Cree also provided information and materials support.

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